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EXAMINER	
LI, AIMEE J	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/631,726	Applicant(s) SINHAROY, BALARAM	
	Examiner Aimee J Li	Art Unit 2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5 and 6*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-20 have been considered. Claims 7 and 12 have been amended as per Applicant's request.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-18 and 20 are rejected under 35 U.S.C. 102(e) as being taught by Zuraski Jr. et al., U.S. Patent Number 6,502,188 (herein referred to as Zuraski).

4. Referring to claim 1, Zuraski has taught a method of generating a global history vector comprising the steps of:

a. Determining if a selected group of instructions contains a branch instruction (Zuraski column 2, lines 26-27; column 4, lines 36-40; column 5, lines 23-67; column 11, lines 2-8; and Figure 1);

b. Maintaining a current global history vector in a shift register when the selected group does not contain a branch instruction (Zuraski column 2, lines 26-27; column 4, lines 36-40; column 5, lines 23-67; and Figure 1). In regards to Zuraski, maintaining a current global history vector is inherent, since the vector is not changed in the shift register unless there is a branch.

c. Shifting a first value into the shift register to generate a second vector if the selected group contains a branch instruction and the branch instruction is predicted as a branch taken (Zuraski column 12, lines 38-42; column 13, lines 7-36; Figure 4; and Figure 5);

d. Shifting a second value into the shift register to generate a second vector when the selected group contains a branch instruction and the selected group does not include a branch instruction predicted as a branch taken (Zuraski column 12, lines 38-42; column 13, lines 7-36; Figure 4; and Figure 5).

5. Referring to claim 2, Zuraski has taught storing the generated value in an entry in a branch instruction queue associated with the selected group of instructions (Zuraski column 10, lines 5-6 and Figure 3).

6. Referring to claim 3, Zuraski has taught the step of correcting the generated vector upon a misprediction comprising the substeps of:

a. Retrieving a selected number of bits of the vector stored from the branch instruction queue into the shift register (Zuraski column 10, lines 49-51; column 13, line 26 to column 14, line 5; Figure 3; Figure 5; Figure 6; and Figure 7); and

b. Shifting an updated history bit into the shift register (Zuraski column 10, lines 49-51; column 13, line 26 to column 14, line 5; Figure 3; Figure 5; Figure 6; and Figure 7).

7. Referring to claim 4, Zuraski has taught wherein the first value comprises a logic 1 and the second value is a logic 0 (Zuraski column 12, lines 38-42; column 13, lines 7-36; Figure 4; and Figure 5).

8. Referring to claim 5, Zuraski has taught wherein the selected group of instructions comprises eight instructions (Zuraski column 12, lines 38-42; column 13, lines 7-36; Figure 4; and Figure 5).

9. Referring to claim 6, Zuraski has taught a method of performing branch predictions comprising the steps of:

a. Indexing a branch history table using a first global history vector associated with a first fetch group of instructions during a first fetch cycle (Zuraski column 1, lines 12-32; column 12, lines 25-32; and Figure 3);

b. Generating a second global history vector associated with a second fetch group of instructions (Zuraski column 13, line 37 to column 14, line 5; Figure 6; and Figure 7) comprising the substeps of:

i. Retaining the first vector when the first fetch group does not contain at least one branch instruction (Zuraski column 2, lines 26-27; column 4, lines 36-40; column 5, lines 23-67; column 11, lines 2-8; and Figure 1);

ii. Appending a bit of a first value to the first vector when the first fetch group has at least one branch instruction predicted to be a branch taken (Zuraski column 12, lines 38-42; column 13, lines 7-36; Figure 4; and Figure 5); and

iii. Appending a bit of a second value to the first vector when the first group contains at least one branch instruction and contains no branch instructions predicted to be a branch taken (Zuraski column 12, lines 38-42; column 13, lines 7-36; Figure 4; and Figure 5); and

c. Indexing the branch history table using the second global history vector during a second fetch cycle to retrieve a second branch prediction value (Zuraski column 1, lines 12-32; column 12, lines 25-32; and Figure 3).

10. Referring to claim 7, Zuraski has taught storing the first and second vectors in an entry of a branch history queue associated with the first fetch group (Zuraski column 10, lines 5-6 and Figure 3).

11. Referring to claim 8, Zuraski has taught

a. Detecting a branch misprediction based on the first prediction value (Zuraski column 10, lines 49-51; column 13, line 26 to column 14, line 5; Figure 3; Figure 5; Figure 6; and Figure 7);

b. Retrieving the first and second vectors from the branch history queue; (Zuraski column 10, lines 49-51; column 13, line 26 to column 14, line 5; Figure 3; Figure 5; Figure 6; and Figure 7)

c. Indexing the branch history table using the first vector to correct the first prediction value (Zuraski column 10, lines 49-51; column 13, line 26 to column 14, line 5; Figure 3; Figure 5; Figure 6; and Figure 7); and

d. Appending a corrected bit to the second vector to generate a corrected branch history vector (Zuraski column 10, lines 49-51; column 13, line 26 to column 14, line 5; Figure 3; Figure 5; Figure 6; and Figure 7).

12. Referring to claim 9, Zuraski has taught wherein said first fetch cycle precedes the second fetch cycle by three fetch cycles (Zuraski column 1, lines 13-20). In regards to Zuraski,

the clock cycle is the shortest possible time interval a stage needs, which includes three fetch cycles.

13. Referring to claim 10, Zuraski has taught wherein said steps of indexing comprises the step of gating the vector with selected bits of a current instruction address (Zuraski column 12, lines 25-38).

14. Referring to claim 11, Zuraski has taught wherein said steps of gating comprise the steps of performing XOR operations (Zuraski column 12, lines 25-38).

15. Referring to claim 12, Zuraski has taught wherein said substeps of appending comprise the substeps of shifting a bit into a shift register storing the second vector (Zuraski column 12, lines 38-42; column 13, lines 7-36; Figure 4; and Figure 5).

16. Referring to claim 13, Zuraski has taught branch processing circuitry comprising:

a. A shift register for storing a global history vector (Zuraski column 9, lines 64-67; column 12, lines 38-42; column 13, lines 7-36; Figure 4; and Figure 5);

b. Control circuitry for selectively updating a first global history vector stored in said shift register (Zuraski column 12, lines 38-42; column 13, lines 7-36; Figure 4; and Figure 5) operable to:

i. Determine if a selected group of instructions contains a branch instruction (Zuraski column 2, lines 26-27; column 4, lines 36-40; column 5, lines 23-67; column 11, lines 2-8; and Figure 1);

ii. Maintain said first global history vector in said shift register when the selected group does not contain a branch instruction (Zuraski column 2, lines 26-27; column 4, lines 36-40; column 5, lines 23-67; and Figure 1).

In regards to Zuraski, maintaining a current global history vector is inherent, since the vector is not changed in the shift register unless there is a branch.

iii. Shift a first value into the shift register to generate a second vector if the selected group contains a branch instruction and the branch instruction is predicted as a branch taken (Zuraski column 12, lines 38-42; column 13, lines 7-36; Figure 4; and Figure 5); and

iv. Shifting a second value into the shift register to generate a second vector when the selected group contains a branch instruction and does not contain a branch instruction predicted as a branch taken.

17. Referring to claim 14, Zuraski has taught a branch history table and circuitry for generating an index to an entry in said branch history table using selected bits from a current address and selected bits of said first vector to retrieve a prediction value stored therein (Zuraski column 1, lines 12-32; column 12, lines 25-32; and Figure 3).

18. Referring to claim 15, Zuraksi has taught circuitry for updating said second vector when said prediction value results in a misprediction comprising:

a. A queue for storing said first and said second vectors (Zuraski column 10, lines 5-6 and Figure 3);

b. Circuitry for accessing said vectors from said queue (Zuraski column 10, lines 5-6 and 49-51; column 13, line 26 to column 14, line 5; Figure 3; Figure 5; Figure 6; and Figure 7);

c. Circuitry for indexing said branch history table with said first vector and updating a corresponding entry with a corrected prediction value (Zuraski column 10, lines 49-51; column 13, line 26 to column 14, line 5; Figure 3; Figure 5; Figure 6; and Figure 7); and

d. Circuitry for updating a vector in said shift register with said second vector (Zuraski column 10, lines 49-51; column 13, line 26 to column 14, line 5; Figure 3; Figure 5; Figure 6; and Figure 7); and

e. Circuitry for shifting the corrected prediction value into said shift register (Zuraski column 10, lines 49-51; column 13, line 26 to column 14, line 5; Figure 3; Figure 5; Figure 6; and Figure 7).

19. Referring to claim 16, Zuraski has taught wherein said branch processing circuitry forms a portion of a single-chip microprocessor (Zuraski column 9, lines 61-63; Figure 1; and Figure 3).

20. Referring to claim 17, Zuraski has taught a processing system comprising:\

a. A microprocessor comprising:

i. A branch history table for storing branch prediction values (Zuraski column 9, lines 34-37; column 10, lines 28-32; and Figure 3);

ii. A global history shift register for storing a global branch history vector (Zuraski column 9, lines 64-67; column 12, lines 38-42; column 13, lines 7-36; Figure 4; and Figure 5);

iii. Logic for generating an index to said branch history table and accessing prediction values stored therein using selected bits of a said branch history

vector stored in said shift register (Zuraski column 1, lines 12-32; column 12, lines 25-32; and Figure 3); and

iv. Control circuitry for updating a said global branch history vector stored in said shift register and operable to:

(1) Retain a current vector stored in said shift register when a selected fetch group does not contain at least one branch instruction (Zuraski column 2, lines 26-27; column 4, lines 36-40; column 5, lines 23-67; and Figure 1). In regards to Zuraski, maintaining a current global history vector is inherent, since the vector is not changed in the shift register unless there is a branch.

(2) Shift a bit of a first value into said shift register to generate an updated vector when the selected fetch group has at least one branch instruction predicted to be a branch taken (Zuraski column 12, lines 38-42; column 13, lines 7-36; Figure 4; and Figure 5); and

(3) Shift a bit of a second value into said shift register when said selected fetch group contains at least one branch instruction and contains no branch instructions predicted to be a branch taken (Zuraski column 12, lines 38-42; column 13, lines 7-36; Figure 4; and Figure 5).

21. Referring to claim 18, Zuraski has taught wherein said microprocessor further comprises:

a. A branch instruction queue having a plurality of entries each associated with a said fetch group for storing at least first and second corresponding global history vectors (Zuraski column 10, lines 5-6 and Figure 3);

b. Circuitry for detecting a misprediction associated with a said prediction value retrieved from said branch history table and corresponding to said first global history vector in said branch instruction queue (Zuraski column 10, lines 49-51; column 13, line 26 to column 14, line 5; Figure 3; Figure 5; Figure 6; and Figure 7);

c. Circuitry for retrieving said first vector from said branch instruction queue and accessing a corresponding entry in said branch history table to correct said prediction value stored therein (Zuraski column 10, lines 49-51; column 13, line 26 to column 14, line 5; Figure 3; Figure 5; Figure 6; and Figure 7); and

d. Circuitry for retrieving and modifying said second vector to generate a corrected vector in said shift register (Zuraski column 10, lines 49-51; column 13, line 26 to column 14, line 5; Figure 3; Figure 5; Figure 6; and Figure 7).

22. Referring to claim 20, Zuraski has taught wherein a said fetch group comprises eight instructions (Zuraski column 4, lines 12-19).

Claim Rejections - 35 USC § 103

23. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

24. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Zuraski Jr. et al., U.S. Patent Number 6,502,188 (herein referred to as Zuraski) as applied to claim 17 above, in view of Jerry M. Rosenberg's Dictionary of Computers, Information Processing, and Telecommunications Second Edition ©1987 (herein referred to as Rosenberg). Zuraski has taught wherein said processing system further includes a bus (Zuraski column 3, lines 59-60 and Figure 1). Zuraski has not explicitly taught system memory coupled to said microprocessor. However, Zuraski has taught that the processor receives instructions from the bus interface unit (Zuraski column 3, lines 59-60). Rosenberg system memory coupled to said microprocessor (Rosenberg page 376, memory (M) (MEM)). A person of ordinary skill in the art at the time the invention was made would have recognized that the system memory stores instructions to the processor, thereby ensuring the instructions are present in the system. Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate the system memory of Rosenberg in the device of Zuraski.

Response to Arguments

25. Applicant's arguments, see paper number 4, filed 04 December 2003, with respect to the rejection(s)of claim(s) 1-20 under Horton et al., U.S. Patent Number 6,223,280 in view of Rahman et al., U.S. Patent Number 5,805,878 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Zuraski Jr. et al., U.S. Patent Number 6,502,188.

Conclusion

26. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure as follows. Applicant is reminded that in amending in response to a rejection of

claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

a. McFarling et al., U.S. Patent Number 5,758,142, has taught a global branch prediction system.

b. Shiell et al., U.S. Patent Number 5,935,241, has taught a branch prediction system with history tables.

c. Talcott, U.S. Patent Number 6,272,623, has taught a global branch prediction system.

d. Baweja et al., U.S. Patent Number 6,332,189, has taught a branch prediction system with a global history register and branch prediction table.

27. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J Li whose telephone number is (703) 305-7596. The examiner can normally be reached on M-T 7:30am-5:00pm.

28. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

29. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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